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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **HATO, Tsunehiro, et al.**

Group Art Unit: **2814**

Serial No.: **10/809,919**

Examiner: **Long PHAM**

Filed: **March 26, 2004**

P.T.O. Confirmation No.: 6752

For: **SUPERCONDUCTING CIRCUIT**

REQUEST FOR RECONSIDERATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

February 22, 2006

Sir:

In response to the Office Action dated **November 29, 2005**, Applicants respectfully request reconsideration of the 35 U.S.C. § 103(a) rejection of claims 1-7 as unpatentable over Applicants' Admitted Prior Art (hereafter, "**AAPA**") in view of U.S. Patent Publication 2004/0077504 to Adachi et al. (hereafter, "**Adachi et al.**").

The Examiner urges **AAPA** teaches that the superconductor or Josephson junction of the single flux quantum circuit requires small hysteresis in the current-voltage characteristic and the superconductor or Josephson junction of the interface circuit requires large hysteresis in the current-voltage characteristic, but fails to teach obtaining the desired current-voltage characteristics or hysteresis of the superconductor or Josephson junction of the single flux quantum circuit and the superconductor or Josephson junction of the interface circuit by changing materials of the junctions or using different materials for the junctions.

The Examiner has cited **Adachi et al.** for teaching that the desired current-voltage

characteristics or hysteresis of superconductor or Josephson junctions can be obtained by using different material for the junctions. See [0048] to [0060].

Applicants respectfully disagree with the Examiner's characteristics of what **AAPA** teaches. Page 2, line 16 to page 3, line 9 disclose that, in **AAPA**, the operation of the SFQ circuit and the operation of the interface circuit are both carried out in a small operational region which compromises performance for both circuits. This passage discloses only that the ideal relation between the critical current density and the operational region is different for each of the SFQ circuit and the interface circuit. This does not suggest that **AAPA** teaches separate Josephson junctions for each of the SFQ circuit and the interface circuit, where the Josephson junctions have different voltage characteristics.

Paragraph [0006] of **Adachi et al.** teaches the ramp edge junctions recited in claims 5-7, but, like **AAPA**, fails to teach, mention or suggest using separate Josephson junctions for each of the SFQ and the interface circuit, as recited in claim 1 of the instant application.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

The Examiner has indicated that claims 8-10 would be allowable if rewritten in independent form. Applicants respectfully defer this action until a FINAL Office Action, if any, is received.

In view of the aforementioned remarks, claims 1-10 are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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